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LID#: P12070**ABSTRACT OF DISCLOSURE**

1 A method of vertically stacking wafers is provided to form three-dimensional (3D) wafer stack. Such
2 method comprising: selectively depositing a plurality of metallic lines on opposing surfaces of adjacent wafers;
3 bonding the adjacent wafers, via the metallic lines, to establish electrical connections between active devices on
4 vertically stacked wafers; and forming one or more vias to establish electrical connections between the active
5 devices on the vertically stacked wafers and an external interconnect. Metal bonding areas on opposing surfaces of
6 the adjacent wafers can be increased by using one or more dummy vias, tapered vias, or incorporating an existing
7 copper (Cu) dual damascene process.
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